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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,203	10/26/2000	Lester J. Kozlowski	24096.00500	3715
7590	09/22/2004		EXAMINER	YE, LIN
Doyle B. Johnson CROSBY, HEAFY, ROACH & MAY P.O. Box 7936 San Francisco, CA 94120-7936			ART UNIT	PAPER NUMBER
			2615	8
DATE MAILED: 09/22/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/697,203	KOZLOWSKI, LESTER J.
	<b>Examiner</b>	<b>Art Unit</b>
	Lin Ye	2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 02 July 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-15 is/are rejected.
- 7) Claim(s) 16 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 26 October 2000 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 7/02/04 have been fully considered but they are not persuasive as to claims 1-15.

For claims 1, 8, 9, and 10, the applicant argues that the Watanabe reference does not have a feedback amplifier. The examiner disagrees. The Watanabe reference discloses in Figure 6, the transistor (103) is successively operated (e.g., the feedback operation successively operated only when the reset transistor 105 is turned on by reset signal) a source follower driver and a feedback amplifier (the drain of transistor 103 connect with drain of the rest transistor 105), connected to an output of the access transistor (102) and to a signal output bus (154 as shown in Figure 1) (See Col. 1, lines 27-42).

The applicant argues the both Watanabe and Kozlowski references does not discloses the photodiode is “directly coupled” to the pixel access transistor (M2). However, this feature is not recited in the claims. The applicant should also note that the Watanabe reference clearly show the photodiode (101) is directly coupled to the drain of the pixel access transistor (102) in Figure 6.

The applicant states “Resetting transistor 102 of Watanabe” in page 8, line 14. This is not corrected. Please noted that the examiner only states the **resetting transistor is 105** and the access transistor is 102 in last office action.

The applicant also argues the combination of Watanabe and Kozlowski is not obvious to one of skill in art, because Watanabe only teaches that fixed pattern noise minimization. The

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examiner disagrees. It is obvious to one of skill in the art to see the advantages for reducing any kind of noises such as fixed pattern noise and rest noise from the image signal to increase the image quality. The Kozlowski reference is an evidence that one of ordinary skill in the art at the time to see more advantages for providing a low noise amplifier system by supplying a tapered reset signal to reset transistor thereby nulling the photodiode reset noise. For that reason, it would have been obvious to modify the system of the Watanabe by providing a tapered reset supply to the reset transistor as taught by Kozlowski for resetting with a tapered reset signal.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S. C. 103(a) as being unpatentable over Watanabe et al. U.S. Patent 6,166,767 in view of Kozlowski et al. International Publication WO 99/53683.

Referring to claim 1, the Watanabe reference discloses in Figures 1,6-9, an active pixel sensor circuit comprising: a photodetector (photoelectric conversion 101); an access

transistor (transfer transistor 102) connected to the photodetector; an electronically reconfigurable transistor (103), successively operated (e.g., the feedback operation successively operated only when the reset transistor 105 is turned on by reset signal) as a source follower driver and a feedback amplifier (e.g., the drain of transistor 103 connect with drain of the rest transistor 105), connected to an output of the access transistor and to a signal output bus (154 as shown in Figure 1); and a reset transistor (105) connected between the access transistor (102) and the amplifier transistor (103) (See Col. 1, lines 27-42, Col. 2, lines 9-10 and Col. 7, lines 62-67). However, the reference does not explicitly shows wherein the reset transistor is reset with a tapered reset signal.

The Kozlowski reference discloses in Figures 4, and 10, an active pixel sensor circuit comprising: reset transistor (16), wherein the reset transistor is reset with a tapered reset signal by tapered reset supply circuit (50). The Kozlowski reference is an evidence that one of ordinary skill in the art at the time to see more advantages for providing a low noise amplifier system by supplying a tapered reset signal to reset transistor thereby nulling the photodiode reset noise. For that reason, it would have been obvious to see the reset transistor is reset with a tapered reset signal disclosed by Watanabe.

Referring to claim 2, the Watanabe reference discloses the CMOS active pixel sensor circuit can have difference configurations. The Kozlowski reference discloses the transistors are MOSFETs. However, the both reference does not explicitly states the transistors are MOSFETs of identical polarity (called Enhancement Mode). Office Notice is taken that both the concept and the advantages of providing the MOSFETs of identical polarity (called Enhancement Mode) transistors in the CMOS active pixel sensor circuit are well known and

expected in the art. It would have been obvious to have the MOSFETs of identical polarity transistors in Kozlowski as these transistors are built without a channel and does not conduct current when  $V_{GS}=0$  (as  $V_{GS}$  changes polarity) and increasing forward bias forms a channel that conducts current (e.g., the applicant's prior art also discloses the MOSFETs of identical polarity transistors in CMOS active pixel sensor circuit as shown in Figure 1).

Referring to claim 3, the Watanabe reference discloses a first column buffer (e.g., including transistors 13, 152, 151 and capacitor 149 in Figure 1) connected (e.g., It should be noted that "connected" means is broad and does not require to show how the first column buffer to connect with rest and electronically reconfigurable transistor.) to the reset (105) and electronically reconfigurable (103) transistors (105 and 103 in Figure 6).

Referring to claim 4, the Watanabe reference discloses a second column buffer (e.g., including transistors 155, 156, 157) connected to signal output bus (OS) as shown in Figure 1.

Referring to claim 5, the Watanabe reference discloses a row disable transistor (row select transistor 104 responses to the pulse voltages  $\Phi_x$ ) connected to the reset transistor (105) as shown in Figure 6 (See Col. 8, lines 19-23).

Referring to claim 6, the Watanabe reference discloses wherein the first column buffer, second column buffer and row disable transistor are connected to a plurality of active pixel sensor circuits as shown in Figure 1.

Referring to claim 7, the Watanabe reference discloses wherein the amplifier transistor operates as a driver of a source follower amplifier (amplification sections 132) when a signal

from the photodetector is being read out on a row-by-row basis, and operates as a driver of a reset amplifier when the photodetector is being reset (See Col. 8, lines 19-28).

Referring to claim 8, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 1.

Referring to claim 9, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 1.

Referring to claim 10, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 1, and the Watanabe reference discloses the access MOSFET (102) having a source connected to the photodetector (101); an amplifier MOSFET (103) having a gate connected to a drain of the access MOSFET (102), and source connected to a signal bus (common signal line 154 in figure 1), and drain connected to a column buffer through VD (the Kozlowski reference also discloses in Figures 5 and 6); and reset MOSFET having a source connected to the drain of the access MOSFET (102), a drain connected to a column buffer through VD and a gate connected to a tapered reset signal generator (the Kozlowski reference also discloses in Figure 4); and a distributed feedback amplifier comprising the amplifier MOSFET (103), the reset MOSFET (105) and the column buffer (e.g., including transistors 13, 152, 151 and capacitor 149 in Figure 1) to a taper reset the photodetector.

Referring to claim 11, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 5, and the Kozlowski reference discloses a row disable MOSFET having a source connected to the drain of the reset MOSFET and a drain connected to a row disable signal generator as shown in Figures 4-6.

Referring to claim 12, the Watanabe reference discloses wherein an access signal generator (the send pulse voltages  $\Phi T$ ) connected to the gate of the access MOSFET (102) in Figure 6.

Referring to claim 13, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 4.

Referring to claim 14, the Watanabe and Kozlowski references disclose all subject matter as discussed with respect to same comment as with claim 2.

Referring to claim 15, the Kozlowski reference discloses wherein the photodetector comprises a substrate diode with the silicide cleared (See Page 9, lines 1-6).

***Allowable Subject Matter***

4. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
  
5. The following is an examiner's statement of reasons for allowance:

The prior art does not teach or fairly suggest the column buffer according to claim 10 comprises: a first switch transistor connected to drain of the reset MOSFET; and a second switch transistor connected to the drain of the amplifier MOSFET; wherein during a reset operation, the first and second switch transistors connect the drain of the reset MOSFET with the drain of the amplifier MOSFET to form a feedback path.

### Conclusion

6. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
  - a. Kuroda et al. U.S 6,469,740 discloses in an image sensor includes a feedback output adjustment section capable of adjusting the potential state of the information storage region.
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, DC. 20231

**Or faxed to:**

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive,  
Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or  
proceeding should be directed to the Technology Center 2600 Customer Service Office  
whose telephone number is (703) 306-0377.



ANDREW CHRISTENSEN  
SUPERVISORY PATENT EXAMINER  
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Lin Ye  
September 14, 2004